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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/706,298 | 11/03/2000 | Frederic Gaillard | AMAT/4564/ISM/LOW K/JW | 6722 |

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| EXAMINER | |
|---|---|
| VINH, LAN | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 1765 | |

DATE MAILED: 11/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/706,298 | GAILLARD ET AL. | |
| | Examiner | Art Unit | |
| | Lan Vinh | 1765 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *25 February 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Shroff et al (US 6,515,343).

Shroff discloses a method for forming a damascene antifuse structure. This method comprises the steps of:

forming a trench in a dielectric layer/material 108 on a surface of a substrate 115 (fig. 7), which reads on forming a feature definition in a dielectric material deposited on a surface of a surface

depositing copper layer 125 /conductive material to fill the trench/feature definition (col 5, lines 7-9; fig. 7)

planarizing the copper layer 125 to expose the dielectric layer/material (col 6, lines 8-10; fig. 8)

etching to remove a portion of the dielectric 108 (col 5, lines 45-47; fig. 6)

forming/depositing a low k dielectric layer 111 (col 4, lines 4-6)

Regarding claims 2, 6, Shroff discloses the steps of: depositing a first dielectric layer 108, depositing second dielectric layer 112 on dielectric 108, depositing third dielectric 109 on dielectric layer 112/second dielectric (col 4, lines 4-7; fig. 9), etching the layer 108, 112 and 109 to form a vertical trench/interconnect (fig. 6), etching the layer 109 to form a trench having a horizontal width, etching to remove a portion of layer 112 exposing layer 108 (fig. 6)

Regarding claims 3, 7, Shroff discloses that dielectric layers 108 and 109 comprises TEOS/oxide (col 4, lines 5-6)

Regarding claims 4, 5, 8, 9, Shroff discloses the dielectric layer 112 (SiN) is an etch stop as seen in fig. 6

Regarding claims 10, 11, Shroff discloses low k layer on the surface of the substrate prior to depositing dielectric layer 109 (fig. 7)

Regarding claims 12-15, Shroff discloses forming a first conductive barrier layer 124 of TiN and a second conductive material of copper 125 on the first conductive material (col 4, lines 1-8, fig. 7)

Regarding claims 16, 17, Shroff discloses the term "low k" is a class of material that has dielectric constant of less than 4.0 (col 5, lines 16-17)

Regarding claims 18, 19, Shroff discloses forming the low k dielectric layer 112 (SiN) prior to forming low k dielectric layer 109 (col 5, lines 22-24; fig. 6)

Regarding claims 20-21, Shroff discloses planarizing the copper layer 125 by CMP after forming low k dielectric layer 108 (col 6, lines 8-10; fig. 8)

Regarding claim 22, fig. 6 of Shroff shows a portion of dielectric layer 108 is etched to the substrate surface

Regarding claims 23, 24, fig. 8 of Shroff shows the dielectric layer 109 adjacent to the horizontal trench is polished

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 25-26, 28-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shroff et al (US 6,515,343) in view of Ning (US 6,323,067).

Shroff discloses a method for forming a damascene antifuse structure. This method comprises the steps of:

forming the dielectric layers 108, and 109 on a surface of a surface (col 4, lines 4-5)

etching the dielectric layers 108 (oxide) and 109 to form a dual damascene definition (fig. 6)

depositing a conductive barrier metal layer 124 (TiN) over the exposed surface of the dual damascene (col 5, lines 3-5)

depositing copper layer 125 /conductive material over the barrier layer 124 to fill the trench/feature definition (col 5, lines 7-9; fig. 7)

planarizing the copper layer 125 and barrier layer 124 to expose the dielectric layer/material (col 6, lines 8-10; fig. 8)

etching to remove a portion of the dielectric 108 (col 5, lines 45-47; fig. 6)

forming/depositing a low k dielectric layer 111 (col 4, lines 4-6)

forming/depositing a dielectric layer 114 (SiN) on the low-k dielectric layer 111 (col 4, lines 6-8; fig. 3)

Shroff differs from the instant claimed invention as per claim 25 by forming a dielectric layer 114 of SiN on the low-k dielectric layer instead of an oxide layer deposited by PECVD /self-planarizing dielectric layer (as defined in page 16 of the specification)

However, Ning, in a method of forming a integrated circuit, discloses that dielectric material such as oxide, SiN can be deposited by PECVD on a low k dielectric layer (col 4, lines 12-16)

Hence, one skilled in the art would have found it obvious to substitute Shroff's SiN dielectric layer with an oxide layer deposited by PECVD /self-planarizing dielectric layer in view of Ning's teaching because Ning discloses that useful preferred dielectric materials include silicon oxide, silicon nitride deposited by PECVD (col 4, lines 11-15), thus the substitution of one for the other would have produced an expected result

Regarding claim 26, Shroff discloses etching the low k dielectric layer to form a dual damascene (fig. 3)

The limitations of claims 28-30 have been discussed above.

Regarding claims 31, 32, Shroff discloses the term "low k" is a class of material that has dielectric constant of less than 4.0 (col 5, lines 16-17)

Regarding claims 35, 36, Shroff discloses forming the low k dielectric layer 112(SiN) prior to forming low k dielectric layer 109 (col 5, lines 22-24; fig. 6)

Regarding claim 40, Shroff discloses planarizing the copper layer 125 by CMP (col 6, lines 8-10; fig. 8)

Regarding claim 33, fig. 6 of Shroff shows a portion of dielectric layer 108 is etched to the substrate surface

Regarding claims 34, fig. 8 of Shroff shows the dielectric layer 109 adjacent to the horizontal trench is polished

Regarding claim 39, Shroff discloses etching the layer 108, 112 and 109 to form a vertical trench/interconnect (fig. 6), etching the layer 109 to form a trench having a horizontal width, etching to remove a portion of layer 112 exposing layer 108 (fig. 6)

5. Claims 27, 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shroff et al (US 6,515,343) in view of Ning (US 6,323,067) and further in view of Zhao et al (US 6,627,539)

Shroff as modified by Ning has been described above. Unlike the instant claimed invention as per claims 27, 43, Shroff and Ning fail to disclose the step of repeating the steps of depositing a conductive barrier layer through the step of planarizing the barrier layer.

However, Zhao discloses a method of forming dual damascene interconnect comprises the step of repeating the steps of depositing a cap barrier layer 304 through the step of planarizing the barrier layer 322 (col 7, lines 25-27)

Since both Shroff and Zhao are concerned with a method of forming dual damascene, one skilled in the art would have found it obvious to modify Shroff and Ning by repeating the steps of depositing a conductive barrier layer through the step of planarizing the barrier layer as per Zhao because Zhao states that it is possible to repeat steps 304-322 to form subsequent dual damascene structure (col 7, lines 27-28)

6. Claims 41-42, 44-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shroff et al (US 6,515,343) in view of Ning (US 6,323,067).

Shroff discloses a method for forming a damascene antifuse structure. This method comprises the steps of:

depositing a first dielectric layer 108, depositing second dielectric layer 112 on dielectric 108, depositing third dielectric 109 on dielectric layer 112/second dielectric (col 4, lines 4-7; fig. 9), etching the layer 108, 112 and 109 to form a vertical trench/interconnect (fig. 6), etching the layer 109 to form a trench having a horizontal width, etching to remove a portion of layer 112 exposing layer 108 (fig. 6)

depositing a conductive barrier metal layer 124 (TiN) over the exposed surface of the dual damascene (col 5, lines 3-5)

depositing copper layer 125 /conductive material over the barrier layer 124 to fill the trench/feature definition (col 5, lines 7-9; fig. 7)

planarizing the copper layer 125 and barrier layer 124 to expose the dielectric layer/material (col 6, lines 8-10; fig. 8)

etching to remove a portion of the dielectric 108 (col 5, lines 45-47; fig. 6)

forming/depositing a low k dielectric layer 111 (col 4, lines 4-6)

forming/depositing a dielectric layer 114 (SiN) on the low-k dielectric layer 111 (col 4, lines 6-8; fig. 3)

Shroff differs from the instant claimed invention as per claim 41 by forming a dielectric layer 114 of SiN on the low-k dielectric layer instead of an oxide layer deposited by PECVD /self-planarizing dielectric layer (as defined in page 16 of the specification)

However, Ning, in a method of forming a integrated circuit, discloses that dielectric material such as oxide, SiN can be deposited by PECVD on a low k dielectric layer (col 4, lines 12-16)

Hence, one skilled in the art would have found it obvious to substitute Shroff's SiN dielectric layer with an oxide layer deposited by PECVD /self-planarizing dielectric layer in view of Ning's teaching because Ning discloses that useful preferred dielectric materials include silicon oxide, silicon nitride deposited by PECVD (col 4, lines 11-15), thus the substitution of one for the other would have produced an expected result

Regarding claim 42, Shroff discloses etching the low k dielectric layer to form a dual damascene (fig. 3)

The limitation of claims 44, 49, 50 have been discussed above.

Regarding claims 45, 46, Shroff discloses the dielectric layer 112 (SiN) is an etch stop as seen in fig. 6

Regarding claims 51, 52, Shroff discloses the term "low k" is a class of material that has dielectric constant of less than 4.0 (col 5, lines 16-17)

Regarding claims 53, 54, Shroff discloses forming the low k dielectric layer 112(SiN) prior to forming low k dielectric layer 109 (col 5, lines 22-24; fig. 6)

Regarding claim 47, fig. 6 of Shroff shows a portion of dielectric layer 108 is etched to the substrate surface

Regarding claims 48, fig. 8 of Shroff shows the dielectric layer 109 adjacent to the horizontal trench is polished

7. Claims 55-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shroff et al (US 6,515,343) in view of Annapragada (US 6,303,525).

Shroff's method has been described above in paragraph 2. Unlike the instant claimed inventions as per claims 55-56, Shroff does not disclose the specific flow rates of the gases, the chamber pressure and substrate temperature during the step of forming the low-k dielectric layer.

Annapragada discloses a method for depositing a low-k dielectric by flowing trimethylsilane gas (10-60 sccm), N2O/oxidizing gas (200-1800 sccm) into a chamber having a pressure of 2-10 Torr at a substrate temperature of 150-400$^0$ C (col 4, lines 15-25)

Hence, ones skilled in the art would have found it obvious to modify Shroff's step of forming the low-k dielectric by using the depositing process parameters as per Annapragada because Annapragada states that depending upon the chemistry of the deposition process, the ratio of silicon-to-oxygen may vary, the process may form silicon rixh oxide (col 3, lines 56-58)

8. Claims 57-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shroff et al (US 6,515,343) in view of Ning (US 6,323,067) and further in view of Annapragada (US 6,303,525).

Shroff as modified by Ning method has been described above. Unlike the instant claimed inventions as per claims 57-60, Shroff and Ning do not disclose the specific flow rates of the gases, the chamber pressure and substrate temperature during the step of forming the low-k dielectric layer.

Annapragada discloses a method for depositing a low-k dielectric by flowing trimethylsilane gas (10-60 sccm), N2O/oxidizing gas (200-1800 sccm) into a chamber having a pressure of 2-10 Torr at a substrate temperature of 150-400$^0$ C (col 4, lines 15-25)

Hence, ones skilled in the art would have found it obvious to modify Shroff and Ning step of forming the low-k dielectric by using the depositing process parameters as per Annapragada because Annapragada states that depending upon the chemistry of the deposition process, the ratio of silicon-to-oxygen may vary, the process may form silicon rixh oxide (col 3, lines 56-58)

***Response to Arguments***

9. Applicant's arguments with respect to claims 1-60 have been considered but are moot in view of the new ground(s) of rejection.

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

***Conclusion***

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan Vinh whose telephone number is 703 305-6302. The examiner can normally be reached on M-F 8:30-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 703 305-2667. The fax phone number for the organization where this application or proceeding is assigned is 703 872-9310.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 308-0661.

LV
November 17, 2003

NADINE G. NORTON
SUPERVISORY PRIMARY EXAMINER